**Final Year Projects**

**Dr Constantinides Final Year Project**

Designed as remote control over wifi

Used with iphone/android tablet

Open API to develop code wjich allows running from arbitrary device – Not tried, unsure of quality

A free libraries allows video stream

Attempt to devise autonomous control, automated take off and landing

Maybe use openCL on android tablet such as Nexus 10

**Data Mining**

Data mining, throw data at algorithm and attempt to get answer to questions unthought-of

Clustering of data

Data nearly clean, but very large – Every state school in the country

Differences in way data is reported dependent upon type of school, academy etc

Python a possibility, but other solutions would be possible

See

1. How far existing datamining solutions can be pushed to find interesting data
   1. How to get data into datamining system
   2. Use tools to try and draw inferences
      1. Social indicators – attainment, wealth
      2. Extract social information from data, or scientific data
2. How could existing datamining solutions be improved to get more useful data
3. How could you encode information into the data mining engines such as axioms which as given knowledge

**Distributed OpenCL**

Take openCL, add another layer of hierarchy.

Allow distribution of OpenCL across multiple OpenCL compliant devices on a network

High value target

Hierarchy of synchronization points for task

Optimization of memory management

Possibility of research idea failure != project failure, can still get good marks

**Sea of CPU’s**

Massive number of logic components and complex DSPs with dual port RAMs on modern FPGAs

Current implementations such as NIOS II are based on classic 5 stage MIPS but are very large

ISA must do enough to be useful

May want to remove classic memories and use message passing

1 DSP, 1 block RAM, some logic. If processor can be small enough, can have 7000 processors on an FPGA

How small, and fast and functional can you make a processor on an FPGA.

If it’s possible, what could the system be used for?

Need to rethink ISA design, not just try ARM or MIPs etc